AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) An intercommunicating apparatus for transmitting a plurality of intercommunicating signals parallel to one another from a first processor unit to a second processor unit of a duplex processor apparatus, said intercommunicating apparatus comprising:

an output driver having

an input side connected to said first processor unit for receiving intercommunicating signals for said first processor and

an output side for transmitting said intercommunicating signals supplied from said first processor unit in the form of a serial signal having a redundancy data structure; and

an input driver having

an input side connected to said output side of said output driver to receive said serial signal having a redundancy data structure and

an output side connected to said second processor unit,

said input driver for receiving said serial signal transmitted from said output driver to reproduce said intercommunicating signals in the form of parallel signals and to supply the reproduced intercommunicating signals, from said

output side, to said second processor unit.

2. (currently amended) An intercommunicating apparatus as claimed in Claim 1, wherein said output driver comprises a coding circuit for producing an error detecting code signal as said serial signal,

said input driver comprises [[an]] a decoding circuit for decoding said error detecting code signal to detect an error on said error detecting code signal, said decoding circuit suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected.

3. (currently amended) An intercommunicating apparatus as claimed in Claim 2, wherein said coding circuit comprises:

a redundancy bit producing circuit connected to said first processor unit for producing at least one redundancy bit on the basis of said intercommunicating signals, and

a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bit(s) in a predetermined cycle to produce said serial signal,

said decoding circuit comprising:

a demultiplexing circuit connected to said multiplexing circuit for demultiplexing said serial signal into received intercommunicating signals and received redundancy bit(s),

[[a]] an error detecting circuit connected to said demultiplexing circuit for detecting an error on said received

intercommunicating signals by the use of said received redundancy bit(s), and

a signal holding circuit connected to said error detecting circuit and said second processor unit for holding said received intercommunicating signals to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit.

4. (original) An intercommunicating apparatus as claimed in Claim 3, wherein said error detecting circuit clears held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said error is detected.

5. (original) An intercommunicating apparatus as claimed in Claim 3, said redundancy bit producing circuit comprises a parity generating circuit for generating a parity bit as said redundancy bit.

6. (original) An intercommunicating apparatus as claimed in Claim 3, said redundancy bit producing circuit uses an error correction code or a cyclic redundancy check code to produce said redundancy bit(s).

7. (original) An intercommunicating apparatus as claimed in Claim 3, said cording circuit further comprises a timing generating circuit connected to said multiplexing circuit for generating a timing signal to decide said predetermined cycle.

8. (original) An intercommunicating apparatus as claimed in Claim 3, said decoding circuit further comprises a timer circuit connected to demultiplexing circuit and said signal holding circuit for clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said demultiplexing circuit does not receive said serial signal for a predetermined time period.

9. (original) An intercommunicating apparatus as claimed in claim 1, said intercommunicating apparatus further comprises:

an additional output driver connected to said second processor unit and having the same structure as said output driver for transmitting additional intercommunicating signals supplied from said second processor unit; and

an additional input driver connected to said additional output driver and said first processor unit and having the same structure as said input driver for reproducing said additional intercommunicating signals to supply the reproduced additional intercommunicating signals to said first processor unit.

10. (currently amended) A method for transmitting a plurality of intercommunicating signals parallel to one another from a first processor unit to a second processor unit of a duplex processor apparatus, said method comprising the steps of:

accepting said intercommunicating signals, together

with a parity signal based on the intercommunicating signals;

changing said intercommunicating signals supplied from said first processor unit and said parity signal into a serial signal having a redundancy data structure;

reproducing said intercommunicating signals and said parity signal in the form of parallel signals from said serial signal; and

supplying the reproduced intercommunicating signals to said second processor unit, said parity signal not being supplied to said second processor unit.

11. (original) A method as claimed in Claim 10, said serial signal comprising an error detecting code signal, said method further comprising the steps of:

detecting an error on said error detecting code signal, and

suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected.

12. (original) A method as claimed in Claim 10, wherein said changing step comprises the steps of:

producing at least one redundancy bit on the basis of said intercommunicating signals, and

multiplexing said intercommunicating signals and said redundancy bit(s) in a predetermined cycle to produce said serial signal,

said reproducing step comprising the steps of:

demultiplexing said serial signal into received intercommunicating signals and received redundancy bit(s),

detecting an error on said received intercommunicating signals by the use of said received redundancy bit(s), and

holding said received intercommunicating signals in a signal holding circuit to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit.

13. (original) A method as claimed in Claim 12, wherein said reproducing step further comprises the step of:

clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said error is detected.

14. (original) A method as claimed in Claim 12, wherein said redundancy bit comprises a parity bit.

15. (original) A method as claimed in Claim 12, wherein said redundancy bit(s) generated by use of an error correction code or a cyclic redundancy check code.

16. (original) A method as claimed in Claim 12, wherein said changing step further comprises the step of:

generating a timing signal to decide said predetermined cycle.

17. (original) A method as claimed in Claim 12, wherein said reproducing step further comprises the steps of:

clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when said serial signal is not received for a predetermined time period.

18. (new) The apparatus of claim 1, wherein,

the intercommunicating signals from said first processor unit are operation mode signals comprising a signal ACTN representative of an active system, a signal SYNC representative of a duplex operation state, and a signal RUNN representative of an execution state.

19. (new) A duplex intercommunicating apparatus for transmitting a plurality of intercommunicating signals parallel to one another from a first processor unit to a second processor unit of a duplex processor apparatus, the intercommunicating apparatus comprising:

an output driver having a serial output; and

an input driver having a serial input serially connected to the serial output of the output driver,

the output driver comprising

a parity generating circuit accepting parallel intercommunicating signals from the first processor unit and outputting, at parallel outputs and as parallel signals, the accepted intercommunicating signals together with a parity signal, the parity signal based on the intercommunicating signals supplied from the first processor,

a timing generator, and

a parallel to serial multiplexer connected to the parallel outputs of the parity generating circuit and accepting the intercommunicating signals and the parity signal output from the parity generating circuit,

the multiplexer outputting, at the serial output of the output driver, a serial signal comprising the intercommunicating signals and the parity signal,

the input driver comprising

a serial to parallel demultiplexer accepting the serial signal from the serial output and reproducing the intercommunicating signals and the parity signal as parallel signals,

a parity checker receiving the parallel signals from the demultiplexer and outputting the intercommunicating signals,

the parity checker for detecting an error on the intercommunicating signals by use of the parity signal,

a state holding circuit having a clear-signal line connected from the parity checker and other lines connected from the parity checker for receiving the intercommunicating signals from the parity checker and holding the intercommunicating signals, as held content, for output to the second processor unit, wherein,

when the parity checker detects an error, the error detecting circuit clears the held content held in state holding

circuit to suspend supply of the intercommunicating signals to the second processor unit when the error is detected.

20. (new) The apparatus of claim 19, wherein,

the intercommunication signals from the first processor unit are operation mode signals comprising

a signal ACTN representative of an active system,

a signal SYNC representative of a duplex operation state, and

a signal RUNN representative of an execution state.